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(54) Integrated controlled power MOSFET.

(57) A semiconductor device is provided which includes a power insulated-gate field effect transistor and a control semiconductor element formed in a common semiconductor substrate (18). A first area (27) is so formed as to provide a drain region of low resistance in the insulated-gate field effect translator and made in resistivity different than a second region (24a, 24b) where the control semiconductor element is formed. It is thus possible to integrate respective elements in a common semiconductor substrate (18), unlike the case where these respective elements are integrated separately into a common semiconductor substrate.

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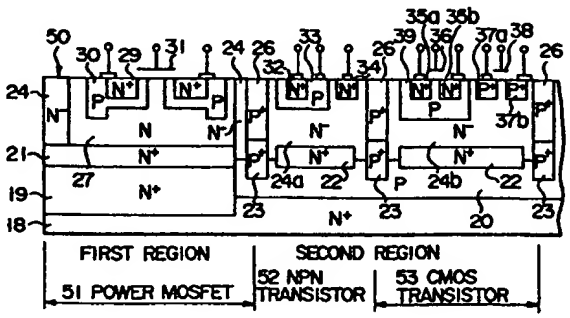


FIG. 2

Semiconductor device

The present invention relates to a semiconductor device which is manufactured by monolithically integrating a Power MOS FET, that is a power insulated-gate type FET having a drain region of high resistance, and a small-signal semiconductor element in a single semiconductor substrate in which the semiconductor element is employed for controlling the Power MOS FET.

An explanation will be given below of one conventional form of a composite semiconductor device manufactured by monolithically integrating in a single semiconductor substrate a Power MOS FET having a drain region of high resistance, NPN transistor; and MOS transistor. Fig. 1 is a cross-sectional view showing a semiconductor device. A Power MOS FET will be explained below by way of example. The semiconductor device as shown in Fig. 1 includes N^+ drain regions (1, 2) having a low resistance, N^- type drain area 3 having a high resistance, P type body 4, N^+ type source region 5 and gate electrode 6. An NPN transistor will be explained below in connection with the semiconductor device shown in Fig. 1. The semiconductor device further includes N^+ type collector region 7 having a low resistance, N^- type collector area 8a having a high resistance, P type base 9, N^+ type emitter 10 and N^+ type collector region from which a collector current is taken out for external connection.

A CMOS transistor will now be given below in connection with the semiconductor device shown in Fig. 1. The semiconductor device further includes the CMOS transistor having N^- type area 8b, p^- type well 12, N^+ type drain region 13a and N^+ type source region 13b of an N channel MOS FET within a p^- type well, gate electrode 15 of an N-channel type MOS FET, p^+ type drain region 14a and p^+ type source region 14b of an FET and gate electrode 16 of a P channel MOS FET. P^+ type regions 17a and P type region 17b provide an electrical isolation, by a PN junction isolation method, among the Power MOS FET, NPN transistor and C-MOS transistor.

According to the conventional technique, drain are 3 having a high resistance in the Power MOS FET, N^- type collector area 8a having a high resistance in the NPN transistor and area 8b in the CMOS FET transistor are simultaneously formed in the semiconductor substrate by an epitaxial growth method. In this way, these regions have the same resistivity, but an optimum resistivity normally differs among the drain region of high resistance in the Power MOS FET, high resistance region in the NPN transistor, and so on. An optimum resistivity value of the drain region having a high resistance in the power MOS FET should be about 1 Ω•cm, for instance, at V_{DSS} = 60V where V_{DSS} represents a maximum drain-to-source voltage at the time of short-circuiting between the gate and source circuits of an associated transistor. On the other hand, an optimum resistivity value of the collector region having a high resistance in the NPN transistor should be about 6 Ω•cm, for instance, at Vz_{CEO} = 60V where V_{CEO} represents a maximum voltage between the collector and the emitter of an associated transistor with a base open-circuited. If the Power MOS FET and NPN transistor are integrated, as a Power-IC, in a single semiconductor substrate, when areas 3 and 8a are so formed as to have a resistivity value fitted for the NPN transistor, then the drain-to-source voltage V_{DSS} of the power MOS FET becomes greater than necessary with the result that the ON resistance per unit area becomes much greater. Thus the area of the power MOS FET necessary to obtain a desired ON resistance becomes much greater than that when an MOS FET is formed as a discrete part, so that there is involved a poor yield. Where areas 3 and 8a are formed with a resistivity value suitable for the Power MOS FET, restriction is imposed on the collector-to-emitter voltage V_{CEO} of the NPN transistor, making it very difficult to achieve a circuit design involved.

If a semiconductor element and Power MOS FET having a drain region of high resistance are to be monolithically formed on a single semiconductor substrate, they are usually formed simultaneously, for example, by an epitaxial growth so that they have the same resistivity value. This resistivity value is properly selected in view of the characteristics of both the elements. In the conventional techniques it is very difficult to make the characteristics of the Power MOS FET within the aforementioned composite semiconductor device, such as the ON resistance and withstand voltage, equal to those of the Power MOS FET manufactured as a discrete element.

This type of composite semiconductor has extensively employed in a quickly expanding application field and there is also a wider demand for the characteristics of elements integrated. It is very important to optimally design integrated elements as mutually independent, discrete ones.

It is accordingly an object of the present invention to provide a composite semiconductor device which is manufactured by monolithically forming a Power MOS FET and control FET on a single semiconductor device such that the characteristics of such integrated elements, such as the power MOS FET in particular, are made equal to those of

an element (Power MOS FET) formed as a discrete element.

In the semiconductor device of the present invention, a Power MOS FET having a drain region of high resistance, as well as a semiconductor element for control, is monolithically formed in a single semiconductor substrate such that the resistance value of a first area of the Power MOS FET, i.e., a drain region of high resistance, and that of a second area of a control transistor element are different from each other.

In the composite semiconductor device of the present invention the resistivity value of the first area of the power MOS FET, i.e., the drain region of high resistivity and that of a second area, i.e., a control element can be made fitted for element formation. The characteristics of respective elements thus integrated can be made equal to those of elements which are formed as discrete elements. The aforementioned feature of the present invention can improve a problem, such as an increase in the ON resistance in particular of the Power MOS FET, which occurs due to the same resistivity involved between a power MOS FET section and a control element section in the conventional composite semiconductor device. Since the area of the Power MOS FET section can be made smaller than that of the conventional semiconductor device, it is thus possible to form semiconductor elements at a low cost in high yield.

Fig. 1 is a cross-sectional view showing a conventional semiconductor device;

Fig. 2 is a cross-sectional view showing a semiconductor device according to one embodiment of the present invention;

Fig. 3(a) to Fig. 3(f) show a process of manufacturing a semiconductor device shown in Fig. 2;

Fig. 4 is a cross-sectional view showing a semiconductor device according to another embodiment of the present invention;

Fig. 5(a) and Fig. 5(b) are cross-sectional views showing another embodiment of the present invention;

Fig. 6(a) and Fig. 6(b) are cross-sectional views showing a semiconductor device according to another embodiment of the present invention;

Fig. 7(a) and Fig. 7(b) are cross-sectional views showing a semiconductor device according to another embodiment of the present invention;

Fig. 8(a) to Fig. 8(f) are cross-sectional views showing a semiconductor device according to another embodiment of the present invention;

Fig. 9 is a cross-sectional view showing a semiconductor device according to another embodiment of the present invention; and

Fig. 10(a) to Fig. 10(c) are cross-sectional views showing a semiconductor device according to another embodiment of the present invention.

The embodiments of the present invention will now be explained below with reference to the accompanying drawings.

Fig. 2 is a cross-sectional view showing a semiconductor device according to a first embodiment of the present invention. Power MOS FET 51, NPN transistor 52 and CMOS transistor 53 used for controlling MOS FET 51 are all integrated in semiconductor substrate 50. Power MOS FET 51 is comprised of high resistance area 27 (first area), a drain region comprised of low resistance regions 18, 19 and 21, P type body 30, and gate electrode 31. NPN transistor 52 used for controlling MOS FET 51 is formed within high resistance N^- type area 24a (second area) and comprised of emitter 32, P type base 33, and N^+ type collector 34. Reference numeral 22 is an N^+ type collector, which serves to lower the collector resistance. CMOS transistor 53 is formed within N^- type area 24b (second area) and comprises an N-channel MOS FET; which includes N^+ type drain 35a, N^+ type source 35b, and gate electrode 36 formed within P type well 39, and P-channel MOS FET; which includes P^+ type drain 37a, P^+ type source 37b, and gate electrode 38 formed within N^- type area 24b. Power MOS FET 51, NPN transistor 52, and MOS transistor 53 are electrically isolated by P type layer 20 and P^+ type layers 23 and 26 (element isolation layers). In the embodiment shown in Fig. 2, a high resistance drain area (first area) in the Power MOS FET has a resistivity value of about 1 Ω•cm and the substrate area (second area) corresponding to control transistor elements has a resistivity value of 5 to 7 Ω•cm, these values being properly set in the formation of transistor elements.

Fig. 3(a) to Fig. 3(f) are cross-sectional views showing a principal process in manufacturing the aforementioned semiconductor device of the present invention. N^+ type silicon substrate 18 of low resistance is prepared with a highly-concentrated antimony doped therein. A highly-concentrated phosphorus is diffused in a low-resistance drain formation section of a Power MOS FET in a gaseous atmosphere of N_2 and O_2 at 1000° to 1100°C for 30 to 120 minutes to form N^+ type region 19 as shown in Fig. 3(a). P type silicon of 7 to 10 Ω (resistivity) is epitaxially grown on the surface of the resultant structure to form a P type silicon layer (element isolation layer) about 20 or 30 μm in thickness and then thermally diffused in a gaseous atmosphere of N_2 and O_2 at 1100° to 1200°C for 12 to 13 hours to form N^+ type region 19 as shown in Fig. 3(b). Antimony is diffused in the portion of the resultant structure in a gaseous

atmosphere of N_2 at 1100°C to 1200°C for 20 to 120 minutes to form N^+ type region 21, corresponding to a low-resistance drain region in the Power MOS FET as well as low-resistance area 22 used as a controlling element. A P^+ type impurity (boron) is diffused for 30 minutes in an element isolation area of a formation portion with a gaseous atmosphere of 1000°C to 1100°C to form element isolation P^+ type layer 23, as shown in Fig. 3(c). Then N^- type silicon layer 24 (phosphorus) is epitaxially grown on the resultant structure so as to have a desired resistivity value and thickness, as shown in Fig. 3(d). In the embodiment of the present invention, an N^- type silicon layer (second layer) is formed which has a resistivity value of 5 to 7 Ω•cm and a thickness of 17 to 20 μm, suitable to the formation of the NPN transistor used for controlling POWER MOS FET. Then a phosphorus ion and an impurity concentration of 1×10^{12} to 1×10^{13} cm^{-2} used to form N type silicon area 27 are injected into the Power MOS FET formation section at an acceleration voltage of 100 keV. A P^+ type impurity (boron) is diffused for four hours into an element isolation area of a formation portion with a gaseous atmosphere of N_2 at 1000° to 1100°C to form element isolation p^+ type layer 26, as shown in Fig. 3(e). The thermal diffusion is achieved in a gaseous atmosphere of N_2 and O_2 at 1100° to 1200°C for 8 hours, so that element isolation P^+ layer 26 reaches element isolation P^+ type layer 23. In this way, island areas 24a, 24b are formed such that they are surrounded with P^+ and P type silicon layers, that is, element isolation P^+ type layers 23 and 26. At this time, N type silicon area 27 extends in the depth direction, as shown in Fig. 3(f). Island areas 24a and 24b are formed as second areas of the controlling element in the substrate, and N type silicon area 27 is formed as a high resistance drain area (first area) in the Power MOS FET. In this embodiment, the phosphorus concentration and diffusion time are so selected as to be about 1 Ω•cm, a value suitable to the Power MOS FET at V_{DSS} = 60V. In this way, the Power MOS FET is formed at area 27 and the NPN transistor (control) and the CMOS transistor are formed at areas 24a and 24b, respectively, as shown in Fig. 2.

In the first embodiment, epitaxial layer 24 which has a resistive value suitable to the formation of NPN transistor (control), is deposited as shown in Fig. 3(d), noting that second areas 24a, 24b are formed in epitaxial layer 24. Area 27 (first area) of Power MOS FET in epitaxial layer 24 is set to have a proper resistivity value by means of an impurity diffusion method, as shown in Fig. (e) and Fig. (f).

Fig. 4 is a cross-sectional view showing a semiconductor device according to a second embodiment of the present invention. In the first embodiment, N. type silicon 27 (first area) reaches low resistance drain region 21 while, in the second embodiment, first area 27 may be of such a type that it does not reach region 21 in which case thermal diffusion is performed in a shorter time than in the first embodiment, as shown in Fig. 4, for example, for 5 hours in a gaseous atmosphere of N_2 and O_2 at 1100° to 1200°C.

Fig. 5(a) and Fig. 5(b) are cross-sectional views showing a semiconductor device according to a third embodiment of the present invention. In the third embodiment, phosphorus is doped into a semiconductor structure to form low resistance drain region 21 in a Power MOS FET and antimony is dopes as an impurity in low resistance collector region 22 in which case, due to a difference in the diffusion coefficient between the phosphorus and antimony, N type silicon area 27 is made to be more shallow than second area 24a. In Fig. 5(a), area 27 is of such a type that it reaches low resistance drain region 21 and, in Fig. 5(b), region 27 does not reach drain region 21.

Fig. 6(a) and Fig. 6(b) are cross-sectional views showing a semiconductor device according to a fourth embodiment of the present invention. In the fourth embodiment, an area including a Power MOS FET is etched to a desired depth.

N type silicon of a desired resistivity value is epitaxially grown onto that etched section to form N type silicon area 27a, at which time the surface of the resultant structure is planarized.

In Fig. 6(a), region 27a is of such a type that it reaches drain region 21 of low resistivity and, in Fig. 6(b), region 27a does not reach drain region 21.

Fig. 7(a) and Fig. 7(b) show a second embodiment according to a fifth embodiment of the present invention. Although in the aforementioned embodiments the drain area of low resistance has been explained as having a varying resistivity value, it is also possible to vary the resistivity value of area 24a in a control element section as the case may be. In Fig. 7(a), control element formation area (second area) 24a is so formed through impurity diffusion as to be made different in resistivity from a Power MOS FET formation area. In Fig. 7(b), the second area is selectively etched in the semiconductor structure and a layer is epitaxially grown on the corresponding area of the semiconductor structure so as to be made different in resistivity from the Power MOS FET formation area.

Fig. 8(a) to Fig. 8(f) are cross-sectional views showing a semiconductor device according to a sixth embodiment of the present invention. In connection with the first to fifth embodiments, an explanation has been made of the semiconductor device in which a source current of a Power MOS FET is taken out from a first major surface side

(the upper surface side) of the semiconductor substrate and a drain current from a second major surface side (the lower surface side) of the semiconductor substrate.

In the embodiment shown in Fig. 8(a) to Fig. 8-(f), source and drain currents of the Power MOS FET are taken from the first major surface side of the semiconductor substrate. In the embodiment shown in Fig. 8 similar reference numerals are employed to designate parts or elements corresponding to those shown in the embodiment of Fig. 2. Reference numeral 40 shows an N^+ drain region for taking out a drain current of the Power MOS FET. The semiconductor device is of such a type that the drain area (first area) of high resistivity is so formed as to be made different in resistance from control element formation area (24a, 24b) and that area 27 reaches the drain region of low resistance. Fig. 8(b) shows a modified form of semiconductor device in which the first area is so formed through impurity diffusion as to be made different in resistivity from areas 24a, 24b and that the first area does not reach drain region 21 of low resistivity. Fig. 8(c) shows a semiconductor device in which, after the etching of the first area, a layer is epitaxially grown on the surface of the resultant semiconductor structure such that it reaches drain region 21 of low resistance with the former made different in resistivity from the latter. Fig. 8(d) shows a form of semiconductor device in which after the etching of the first area a layer is epitaxially grown on the surface of the resultant structure such that it does not reach the drain region of low resistance. Fig. 8(e) shows a semiconductor device in which a second region is so formed through impurity diffusion as to vary its resistivity value and Fig. 8(f) shows a semiconductor device in which a second area varies its resistivity value by an etching step and epitaxially growing step. Although, in order to make the first and second areas different in resistivity from each other, the N^- type are of high resistance having a lower impurity concentration is converted to the N type area of high impurity concentration in the aforementioned embodiments, the N type area may be changed to the N^- type area either by varying their resistivity values through the diffusion of an impurity of the opposite conductivity type or by etching the N type area and epitaxially growing an N^- type silicon layer of a lower impurity concentration.

Fig. 9 is a cross-sectional view showing a semiconductor device according to a seventh embodiment of the present invention. In the seventh embodiment, after the formation of N type epitaxial layer 24 (see Fig. 3), an impurity (boron) of the other conductivity type is diffused into area 27 in a Power MOS FET to form N type area 27 as N^- type region 40.

The present invention can also be applied to Power MOS FET in another element isolation structure.

Fig. 10(a) to Fig. 10(c) show additional semiconductor devices according to the present invention, that is, a device fabricated by a PN isolation method, device fabricated by a self isolation method and device fabricated by a dielectric isolation method, respectively.

Claims

1. A semiconductor device including a power insulated-gate field effect transistor and control semiconductor element formed in a common substrate, characterized in that:

a first area (27) is so formed as to provide a drain region of high resistance in the power insulated-gate field effect transistor, said first area having a predetermined resistivity value; and

a second area (24a, 24b) is so formed as to provide the control semiconductor element having a resistivity value different from said predetermined resistivity value.

2. A semiconductor device according to claim 1, characterized in that said power insulated-gate field effect transistor is of such a type that a source current is taken from a first major surface side of said semiconductor substrate (18) and a drain current is taken from a second major surface side of said semiconductor substrate (18) which is situated on a side opposite to a side where said first major surface is situated.

3. A semiconductor device according to claim 1, characterized in that said power insulated-gate field effect transistor is of such a type that source and drain currents are taken from a first major surface side of said semiconductor substrate (18).

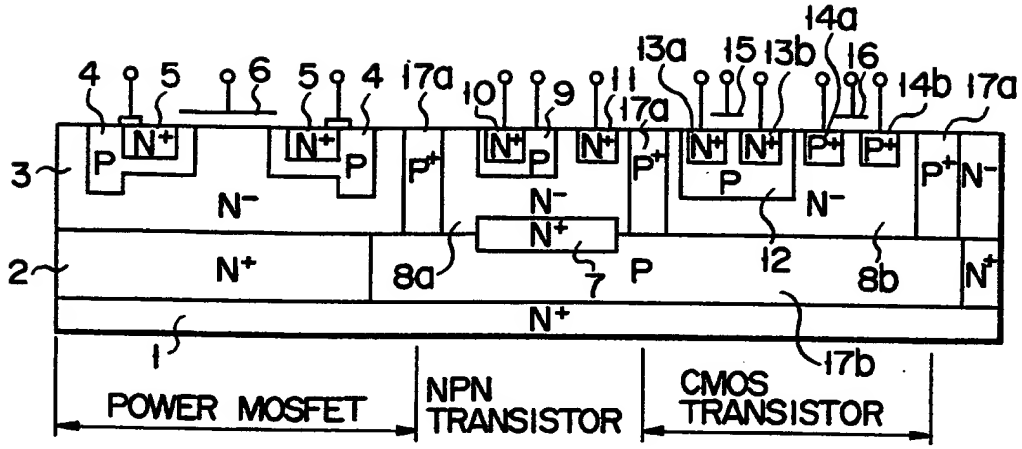
4. A semiconductor device according to claim 1, characterized in that said first area (27) is formed by selectively etching an area where said power insulated-gate field effect transistor is formed and forming a layer at that area by an epitaxial growth method.

5. A semiconductor device according to claim 1, characterized in that said second area (24a, 24b) is formed by selectively etching an area where said control semiconductor element is formed and forming a layer at that area by an epitaxial growth method.

6. A semiconductor device according to claim 1, characterized in that one of said first area (27) and said second area (24a, 24b) is impurity-diffused so as to be made different in resistivity from the other area.

7. A semiconductor device according to claim 1, characterized in that said first area (27) in said power insulated-gate field effect transistor is formed such that it is in contact with a drain region (21) of low resistance in said field effect transistor.

8. A semiconductor device according to claim 1, characterized in that said first gate (27) in said power insulated-gate field effect transistor is of such a type that it is not in contact with a drain region (21) of low resistance in said field effect transistor.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10
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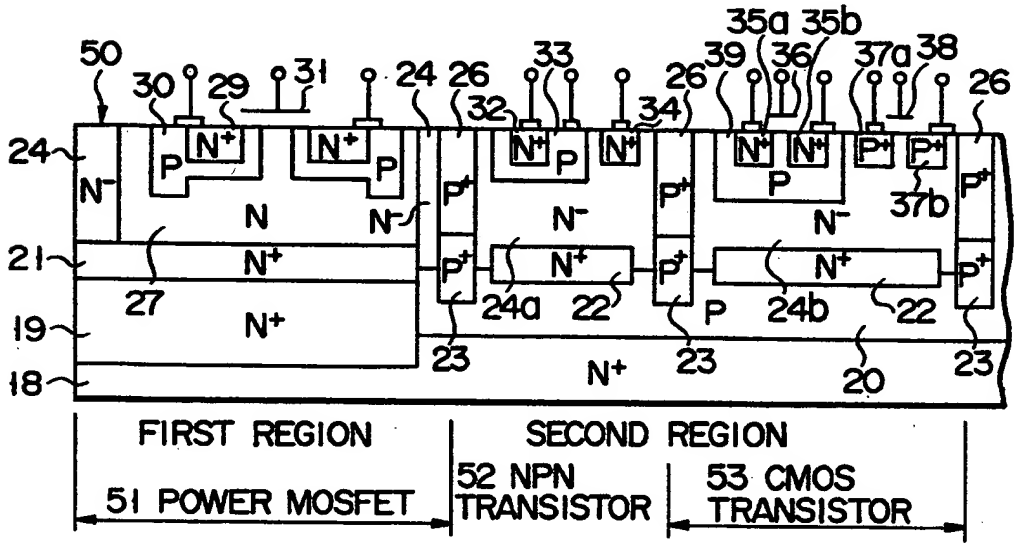
11
17a
13a
15
13b
14a
16
14b
17a
3
2
1
N+
N-
P
P+
8a
7
12
8b
17b
POWER MOSFET
NPN TRANSISTOR
CMOS TRANSISTOR

FIG. 1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35a
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19
18
N+
N-
P
P+
N
27
24a
22
23
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24b
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37b
FIRST REGION
SECOND REGION
51 POWER MOSFET
52 NPN TRANSISTOR
53 CMOS TRANSISTOR

FIG. 2

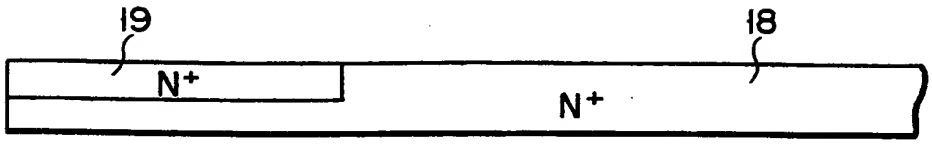


FIG. 3(a)

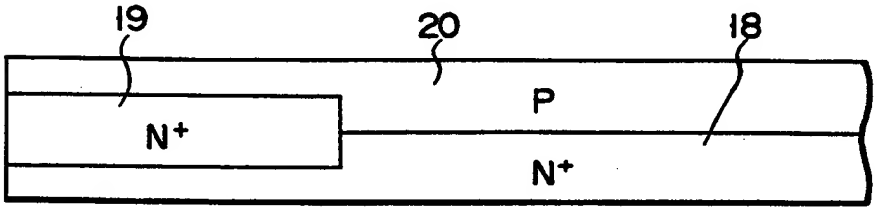


FIG. 3(b)

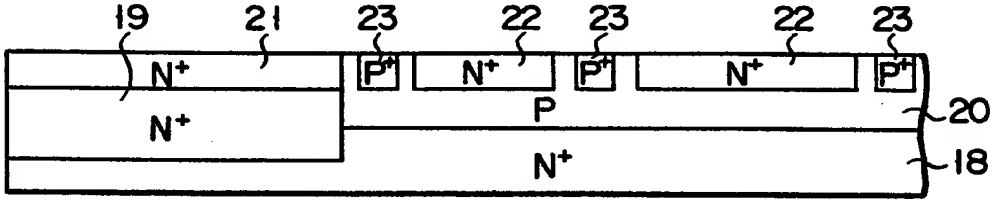


FIG. 3(c)

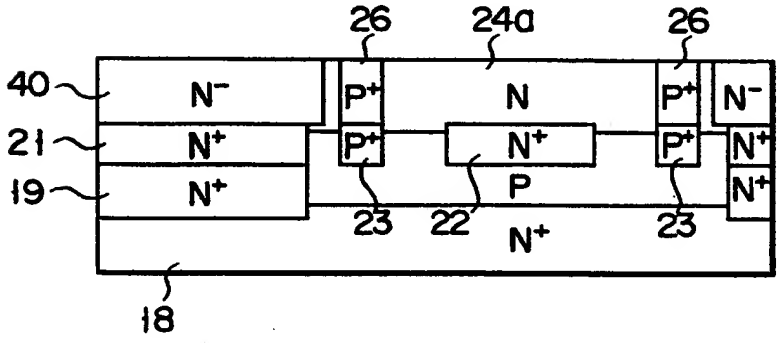


FIG. 9

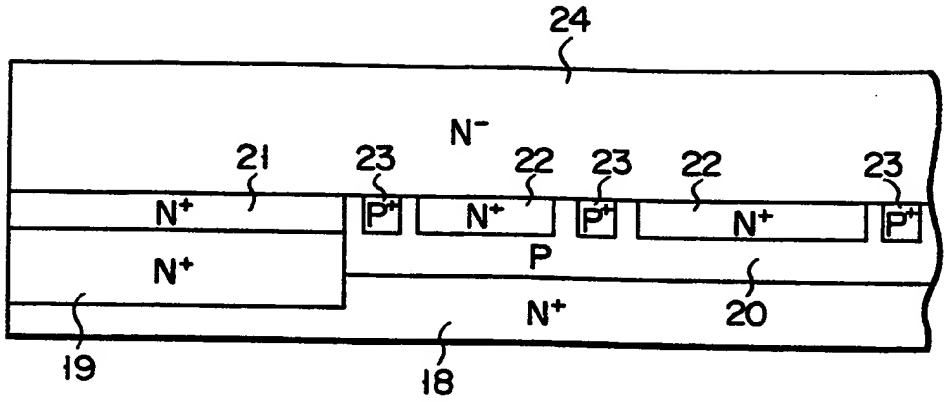


FIG. 3(d)

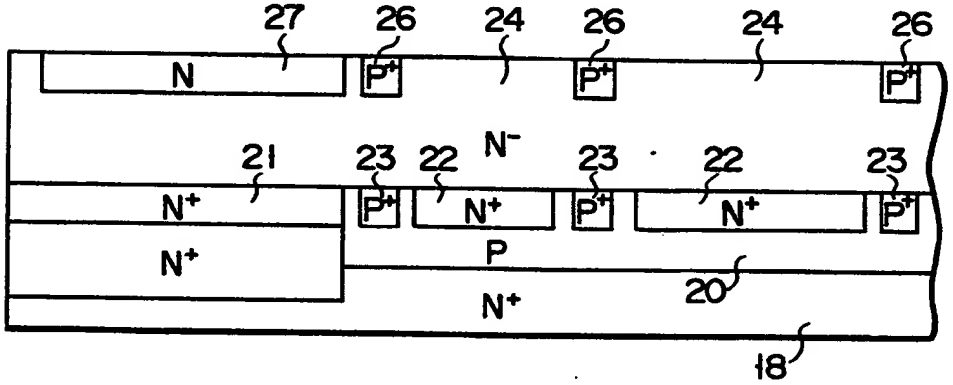


FIG. 3(e)

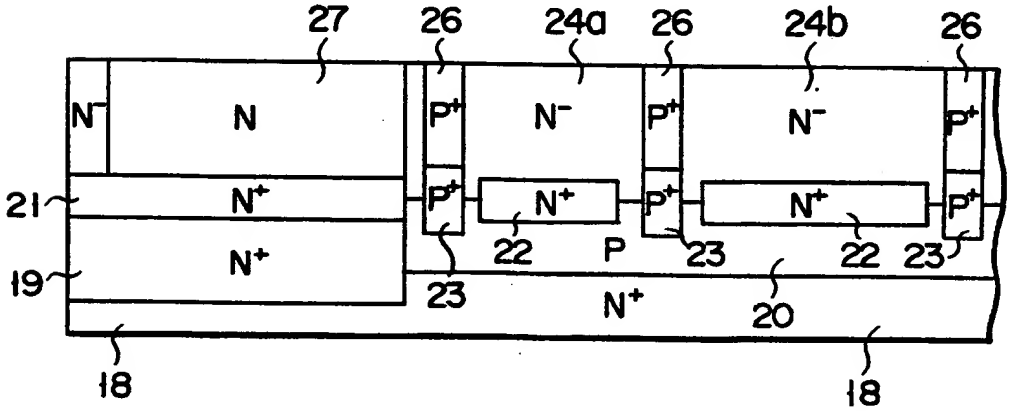


FIG. 3(f)

FIG. 4

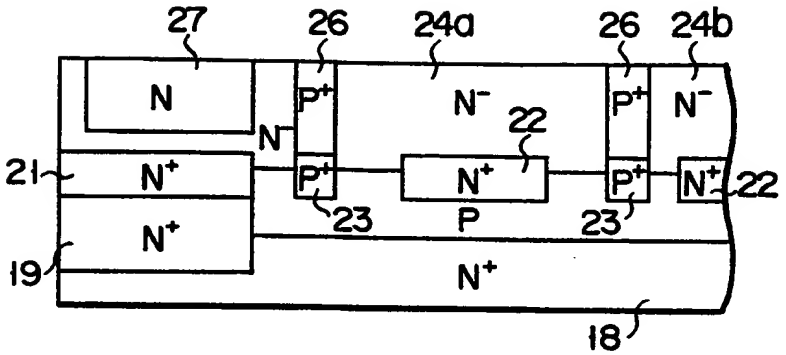


FIG. 5(a)

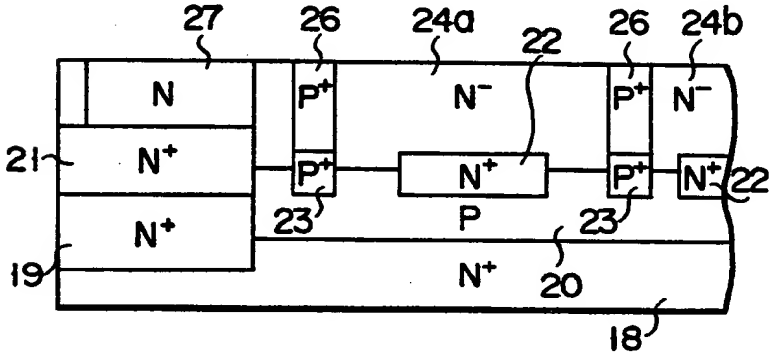


FIG. 5(b)

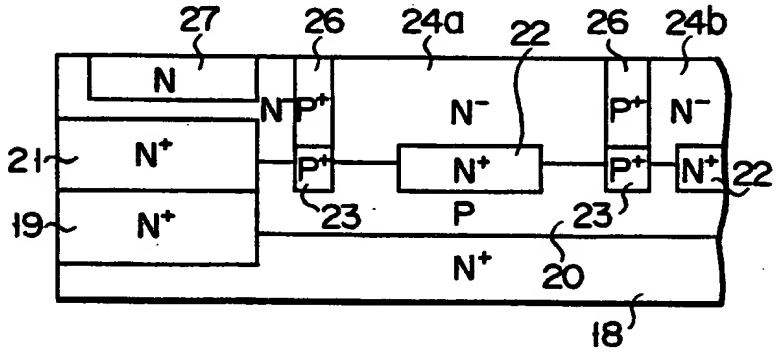


FIG. 6(a)

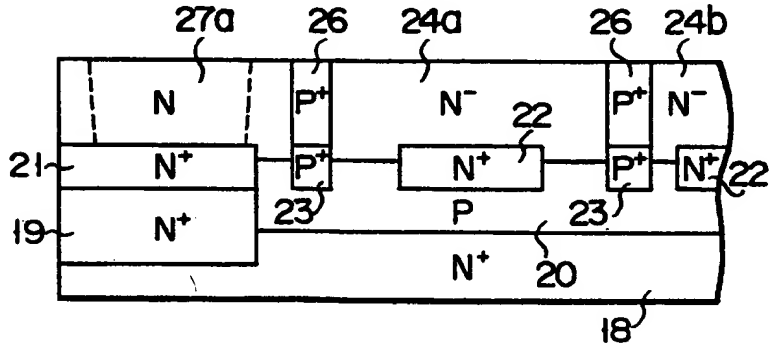


FIG. 6(b)

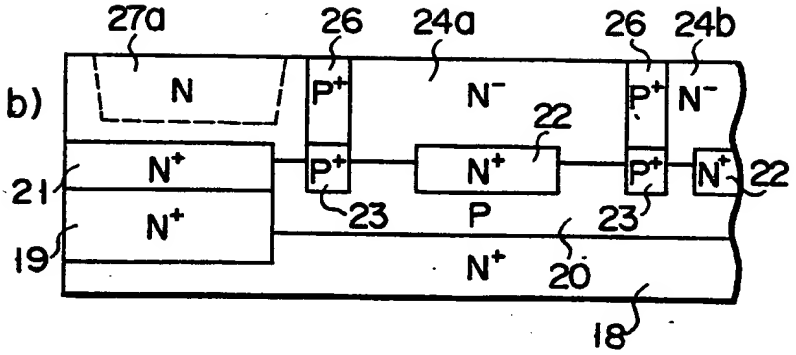


FIG. 7(a)

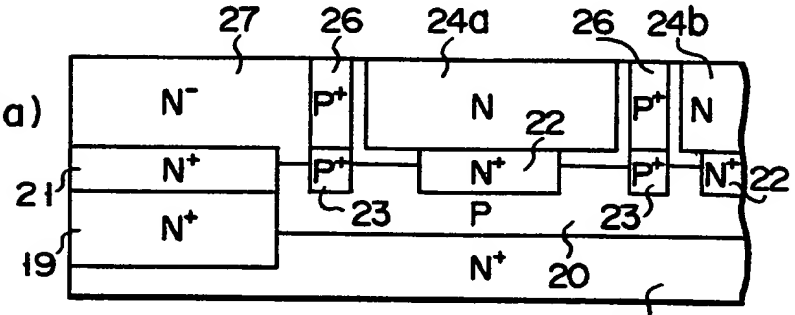
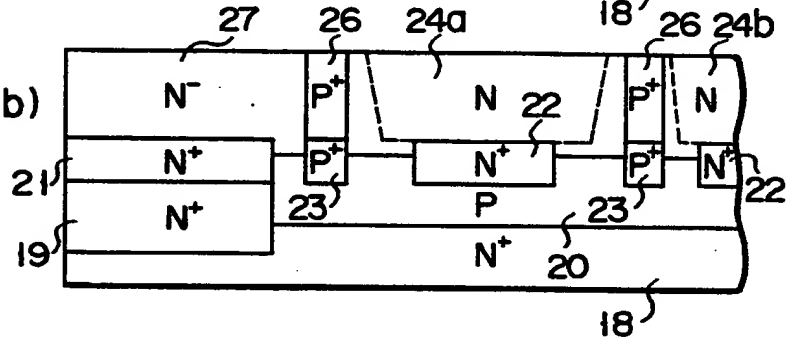


FIG. 7(b)



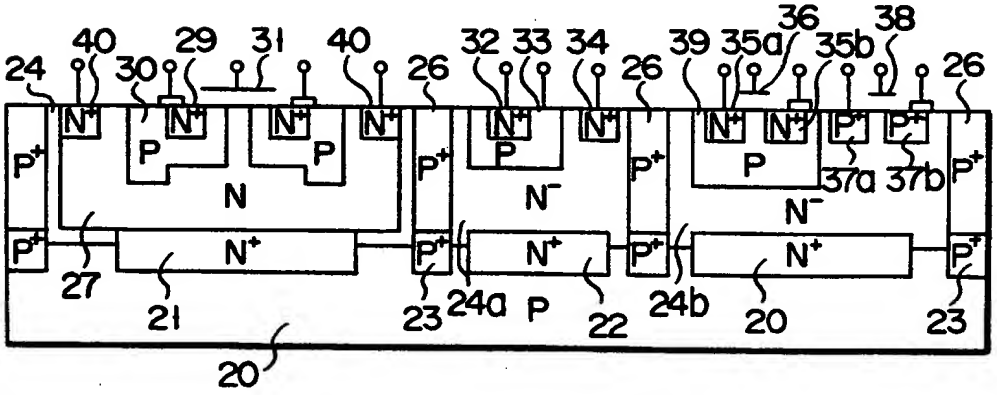


FIG. 8(a)

FIG. 8(b)

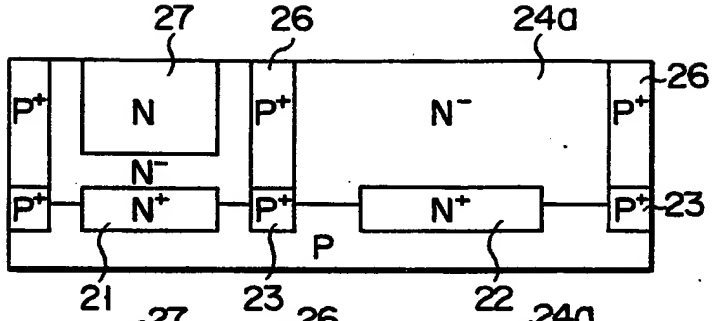


FIG. 8(c)

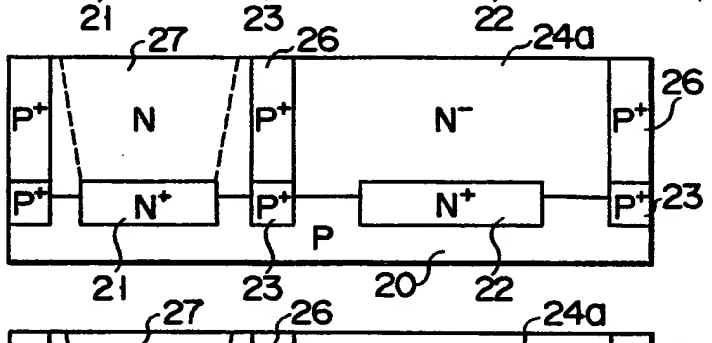


FIG. 8(d)

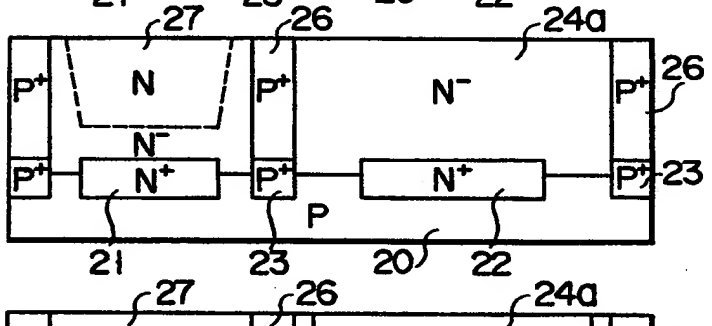


FIG. 8(e)

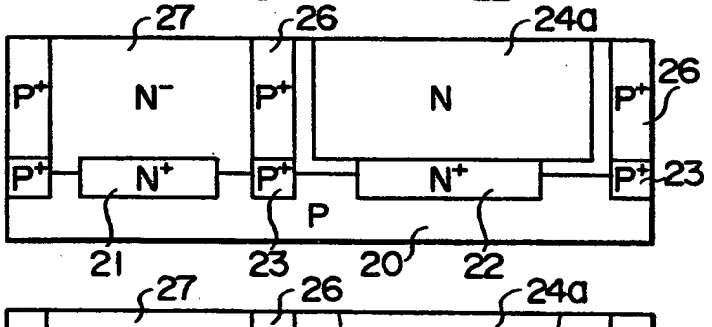
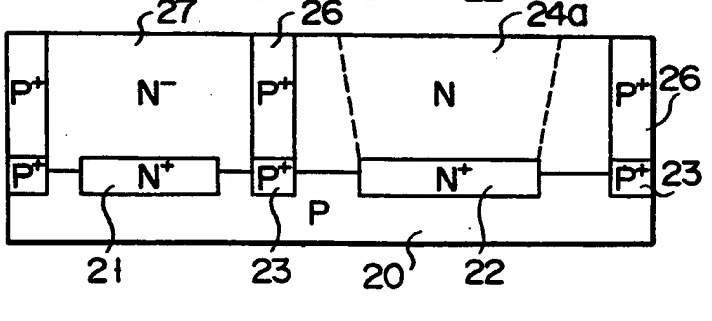


FIG. 8(f)



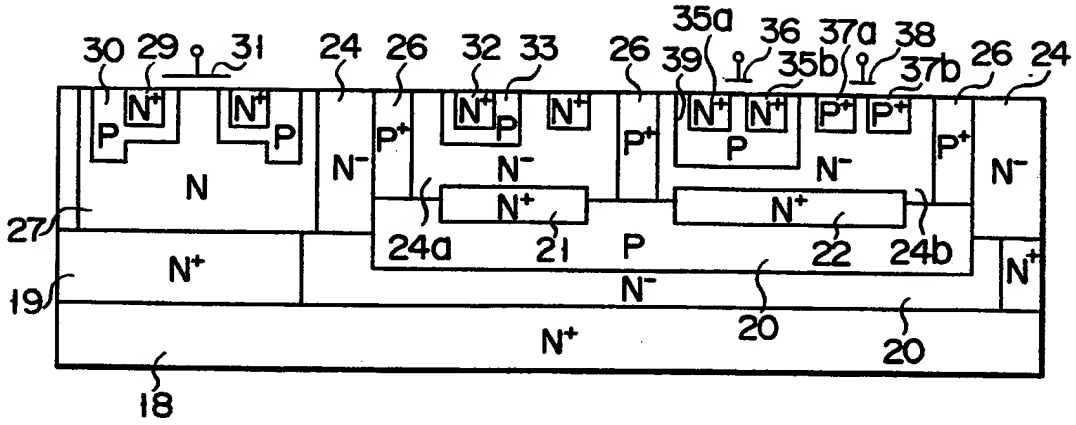


FIG. 10 (a)

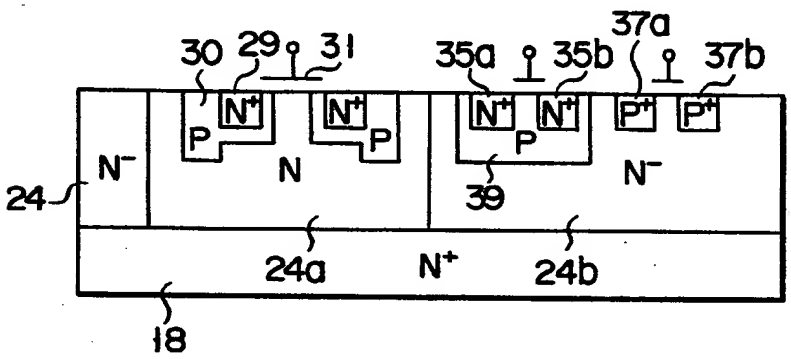


FIG. 10 (b)

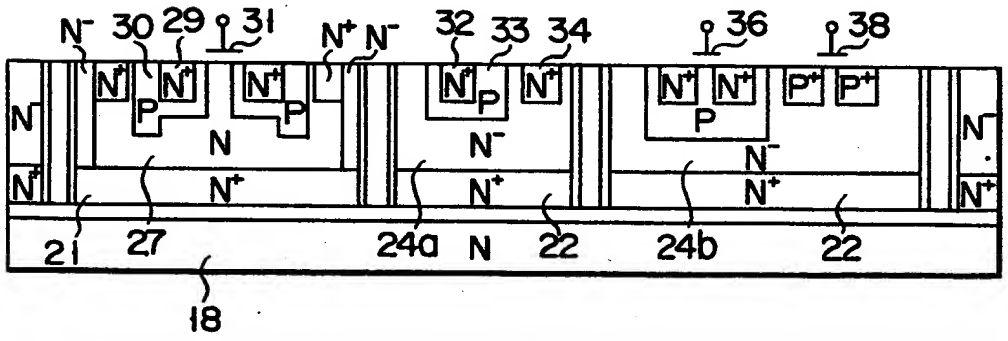


FIG. 10 (c)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 10 1996

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	ELECTRONIC DESIGN, no. 4, 21st February 1985, pages 191-196, Hasbruck Heights, New Jersey, US; W. SCHULTZ et al.: "Mixed MOS devices unite in a switch chip that links power with smarts" * page 193, column 1-3, figure * ---	1,2	H 01 L 27/06
A	PATENT ABSTRACTS OF JAPAN, vol. 8, no. 53 (E-231)[1490], 9th March 1984; & JP - A - 58 206 153 (DAINI SEIKOSHA K.K.) 01-12-1983 * abstract, figure * ---	1,2,6,7	
A	IEEE SPECTRUM, no. 1, January 1985, pages 60-64, New York, US, "In smarter design and fabrication of IC s, power and logic are mixed on the same chip and circuits are integrated over an entire wafer" * figure 1 * -----	3	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	24-03-1988	JUHL A.

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